WHAT IS CLAIMED IS:

1. A method of manufacturing a solder bump connecting a semiconductor chip to a mounting substrate, comprising:

forming a first protrusion extending upwardly from a contact pad on the semiconductor chip;

forming a second protrusion extending upwardly from a ball pad on the mounting substrate; and

embedding the first and second protrusions in a solder material.

2. A method of manufacturing a solder bump according to claim 1, wherein:

at least one of the first and second protrusions are formed primary from a metal or a mixture of metals.

3. A method of manufacturing a solder bump according to claim 1, wherein:

both of the first and second protrusions are formed primary from a metal or a mixture of metals.

4. A method of manufacturing a solder bump according to claim 1, wherein:

the first protrusion includes a plurality of first protrusions arranged on the contact pad.

5. A method of manufacturing a solder bump according to claim 4, wherein:

the plurality of first protrusions are arranged in a substantially parallel orientation.

6. A method of manufacturing a solder bump according to claim 5, wherein:

the plurality of first protrusions are substantially normal to a plane defined by an upper surface of the contact pad.

7. A method of manufacturing a solder bump according to claim 6, wherein:

the plurality of first protrusions includes at least one first protrusion recessed relative to another first protrusion.

8. A method of manufacturing a solder bump according to claim 6, wherein:

the first protrusions have a substantially oval or circular cross-sections.

9. A method of manufacturing a solder bump according to claim 6, wherein:

a portion of at least one first protrusion surrounds at least a portion of a second protrusion.

10. A method of manufacturing a solder bump according to claim 9, wherein:

the surrounding first protrusion has a substantially cylindrical shape.

11. A method of manufacturing a solder bump according to claim 1, wherein:

the second conductive protrusion includes a plurality of second protrusions arranged on the ball pad.

12. A method of manufacturing a solder bump according to claim 11, wherein:

the plurality of second protrusions are arranged in a substantially parallel orientation.

13. A method of manufacturing a solder bump according to claim 12, wherein:

the plurality of second protrusions are substantially normal to a plane defined by an upper surface of the ball pad.

14. A method of manufacturing a solder bump according to claim 13, wherein:

the second protrusions include at least one second protrusion that is recessed relative to another second protrusion.

15. A method of manufacturing a solder bump according to claim 13 wherein:

a portion of at least one second protrusion surrounds at least a portion of a first protrusion.

16. A method of manufacturing a solder bump according to claim 15, wherein:

the surrounding second protrusion has a substantially cylindrical shape.

17. A method of manufacturing a solder bump according to claim 11, wherein:

the second protrusions have a substantially oval or circular cross-sections.

18 A method of manufacturing a solder bump according to claim 1, further comprising:

forming the contact pad on a semiconductor substrate;

forming an under bump metal (UBM) layer on the contact pad, the UBM layer including both a metal adhesion layer formed directly on the contact pad and a metal wetting layer on the metal adhesion layer; and only then

forming the first protrusion on the metal wetting layer.

19. A method of manufacturing a solder bump according to claim 18, wherein:

the UBM also includes a metal oxidation protection layer formed over the metal wetting layer.

20. A method of manufacturing a solder bump according to claim 2, wherein:

the metal or metal mixture is selected from a group consisting of Ni, Cu, Pd, Pt and alloys thereof.

21. A method of manufacturing a solder bump according to claim 1, wherein:

the solder material is selected from the group consisting of Sn, Pb, Ni, Au, Ag, Cu, Bi and alloys thereof.

22. A method of manufacturing a solder bump according to claim 1, further comprising:

depositing an intermediate layer over the contact pad;

forming a photoresist pattern on a surface of the intermediate layer, the photoresist pattern including an opening that exposes a portion of a surface of the intermediate layer;

filling the opening with a conductive material; removing the photoresist pattern to form a first protrusion extending upwardly from the surface of the intermediate layer; and

embedding the first protrusion in a solder material formed over the intermediate layer.

23. A method of manufacturing a solder bump according to claim 22, wherein:

embedding the first protrusion in a solder material includes:

forming a second photoresist pattern, the photoresist pattern including a second opening that exposes the first protrusion and an adjacent surface portion of a solder bump region on the intermediate layer;

filling the second opening with a solder material;

removing the second photoresist pattern; and

reflowing the solder material to embed the first protrusion in a solder bump.

24. A method for manufacturing a solder bump according to claim 1, comprising:

depositing an intermediate layer on the contact pad;

forming a photoresist pattern on the intermediate layer, the photoresist pattern defining an opening that exposes a portion of a surface of the intermediate layer;

filling the opening with a first conductive material to a first depth, thereby forming a shallow opening;

filling the shallow opening with a second conductive material to a second depth, whereby the first and second conductive materials cooperate to fill the opening substantially completely; and

removing the photoresist pattern.

25. A method for manufacturing a solder bump according to claim 24, wherein:

the first conductive material is a metal composition having a melting point above about 300 °C.,

the second conductive material is a solder composition having a melting point at below about 300 °C.

26. A method for manufacturing a solder bump according to claim 24, further comprising:

reflowing the second conductive material, the second conductive material having a volume sufficient to surround the first conductive material, the first conductive material serving as a first protrusion.

27. A method for manufacturing a solder bump according to claim 25, wherein:

the first conductive material is selected from a group consisting of Ni, Cu, Pd, Pt and mixtures and alloys thereof.

28. A method for manufacturing a solder bump according to claim 27, wherein:

the second conductive material is selected from a group consisting of Sn, Pb, Ni, Au, Ag, Cu, Bi and mixtures and alloys thereof.

29. A solder bump structure providing electrical and mechanical connection between a semiconductor chip and a mounting substrate, comprising:

a contact pad arranged on the semiconductor chip;

a first protrusion extending upwardly from the contact pad;

a ball pad arranged on the mounting substrate;

a second protrusion extending upwardly from the ball pad;

a volume of solder material embedding the first and second protrusions.

30. A solder bump structure according to claim 29, further comprising:

an intermediate layer formed on the contact pad;

a plurality of first protrusions; and

a plurality of second protrusions, wherein the volume of solder material is sufficient to embed substantially all of the first and second protrusions.

31. A solder bump structure according to claim 30, wherein:

a portion of a first protrusion overlaps a portion of a second protrusion.

32. A solder bump structure according to claim 30, wherein:

a portion of each of the first protrusions overlaps a portion of each of the second protrusions.

33. A solder bump structure according to claim 29, wherein:

a portion of a first protrusion surrounds a portion of a second protrusion.

34. A solder bump structure according to claim 30, wherein:

a portion of the plurality of the first protrusions are arranged to form a periphery around a portion each of the second protrusions.

35. A solder bump structure according to claim 29, wherein:

a portion of a first protrusion surrounds a portion of a second protrusion;

a portion of the second protrusion surrounds a portion of another first protrusion.

36. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate, the solder bump connection having a central longitudinal axis that is substantially normal to main surfaces of both the semiconductor chip and the mounting substrate, comprising;

preparing a semiconductor chip, the semiconductor chip including a chip pad;

forming a first conductive protrusion on the chip pad;

forming a solder ball on the chip pad, the solder ball encompassing the conductive protrusion;

preparing a mounting substrate, the mounting substrate including a ball pad;

forming a second conductive protrusion on the ball pad;

positioning the solder ball adjacent the second conductive protrusion;

reflowing the solder ball to form the solder bump connection, the solder bump connection encompassing both the first conductive protrusion and the second conductive protrusion, wherein the first and second conductive protrusions are arranged substantially symmetrically about the longitudinal axis.

37. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 36, wherein:

forming the first conductive protrusion includes

forming a first photoresist layer on the semiconductor chip and the chip pad;

patterning the first photoresist layer to form a photoresist pattern having an opening above a portion of the chip pad;

filling at least a portion of the opening with one or more conductive materials; and

removing the first photoresist layer.

38. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 37, wherein:

the conductive material includes a metal selected from a group consisting of Ni, Cu, Pd, Pt and Au; and

the opening is filled by electroplating the conductive material onto the chip pad.

39. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 38, wherein:

forming the first conductive protrusion further includes

forming a second photoresist layer after removing the first photoresist layer;

patterning the second photoresist layer to expose the first conductive protrusion and a portion of the chip pad;

depositing a cover layer of another conductive material on the first conductive protrusion and the exposed portion of the chip pad.

40. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 36, wherein:

forming the second conductive protrusion includes

forming a first photoresist layer on the mounting substrate and the ball pad;

patterning first photoresist layer to form a photoresist pattern having an opening above a portion of the ball pad;

filling at least a portion of the opening with a conductive material; and

removing the first photoresist layer.

41. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 40, wherein:

the conductive material includes a metal selected from a group consisting of Ni, Cu, Pd, Pt and Au; and

opening is filled by electroplating the conductive material onto the chip pad.

42. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 41, wherein:

forming the first conductive protrusion further includes

forming a second photoresist layer after removing the first photoresist layer;

patterning the second photoresist layer to expose the first conductive protrusion and a portion of the chip pad;

depositing a cover layer of a second conductive material on the first conductive protrusion and the exposed portion of the chip pad.

43. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 36, wherein:

the solder connection has a final height T_f;

the first conductive protrusion has a height T_{p1};

the second conductive protrusion has a height T_{p2}; and wherein

the relationship $T_{p1} + T_{p2} < T_f$ is satisfied.

44. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 36, wherein:

the solder connection has a final height T_f;

the first conductive protrusion has a height T_{p1};

the second conductive protrusion has a height T_{p2}; and wherein

the relationship $T_{p1} + T_{p2} \geq T_f$ is satisfied.

45. A method of forming a solder bump connection between a semiconductor chip and a mounting substrate according to claim 44, wherein:

the relationship $T_{p1} + T_{p2} > T_f$ is satisfied; and

a lower portion of the first conductive protrusion surrounds an upper portion of the second conductive protrusion.

46. A method of forming a solder connection between a semiconductor chip and a mounting substrate according to claim 44, wherein:

the relationship $T_{p1} + T_{p2} > T_f$ is satisfied;

the first conductive protrusion includes a plurality of substantially identical protrusions arranged in a first pattern that is substantially symmetrical about the axis; and

the second conductive protrusion includes a plurality of substantially identical protrusions arranged in a second pattern that is substantially symmetrical about the axis.

47. A method of forming a solder connection between a semiconductor chip and a mounting substrate according to claim 46, wherein:

the first conductive protrusions in the first pattern are spaced substantially symmetrically with respect to adjacent protrusions of the second pattern.

48. A method of forming a solder connection between a semiconductor chip and a mounting substrate according to claim 46, wherein reflowing the solder ball further includes:

establishing an initial spacing S_i between the semiconductor chip and the mounting substrate;

heating the solder ball to a temperature sufficient to allow the solder to reflow;

allowing the semiconductor chip and mounting substrate to self-align;

establishing a final spacing S_f between the semiconductor chip and the mounting substrate, the final spacing S_f being smaller than the initial spacing S_i; and

cooling the solder to form the solder connection.

49. A method of forming a solder connection between a semiconductor chip and a mounting substrate according to claim 48, wherein:

the first conductive protrusion has a height T_{p1};

the second conductive protrusion has a height T_{p2}; and wherein

the relationships $T_{p1} + T_{p2} < S_i$ and $T_{p1} + T_{p2} \geq S_f$ are satisfied.

50. A semiconductor device including a semiconductor chip and a mounting substrate interconnected by a solder connection having a central longitudinal axis that is substantially

normal to main surfaces of both the semiconductor chip and the mounting substrate, the solder connection comprising:

solder;

a first reinforcing structure, the first reinforcing structure extending into the solder from the semiconductor chip and substantially contained within the solder; and

a second reinforcing structure. the second reinforcing structure extending into the solder from the mounting substrate and substantially contained within the solder,

wherein the first and second reinforcing structures are arranged substantially symmetrically about the longitudinal axis of the solder connection.

51. A semiconductor device according to claim 50, wherein:

the solder connection has a height T_s;

the first reinforcing structure has a height T_{r1};

the second reinforcing structure has a height T_{r2}; and wherein

the ratio $(T_{r1} + T_{r2}) : T_s$ is between about 1:10 and 1:1.

52. A semiconductor device according to claim 50, wherein:

the solder connection has a height T_s;

the first reinforcing structure has a height T_{r1};

the second reinforcing structure has a height T_{r2}; and wherein

the relationship $T_{r1} + T_{r2} \geq T_s$ is satisfied.

53. A semiconductor device according to claim 52, wherein:

the relationship $T_{p1} + T_{p2} > T_f$ is satisfied; and

a lower portion of the first reinforcing structure surrounds an upper portion of the second reinforcing structure.

54. A semiconductor device according to claim 52, wherein:

the relationship $T_{p1} + T_{p2} > T_f$ is satisfied;

a lower portion of an outer portion of the first reinforcing structure surrounds an upper portion of the second reinforcing structure; and

the upper portion of the second reinforcing structure surrounds a lower portion of an inner portion of the first reinforcing structure.

55. A semiconductor device according to claim 52, wherein:

the first reinforcing structure has a substantially uniform cross-section area along the majority of height T_{p1}.

56. A semiconductor device according to claim 52, wherein:

the second reinforcing structure has a substantially uniform cross-section area along the majority of height T_{p2}.

57. A semiconductor device according to claim 52, wherein:

the cross-section area of the first reinforcing structure and the cross-section area of the second reinforcing structure are substantially equal.

58. A semiconductor device according to claim 52, wherein:

the first reinforcing structure and the second reinforcing structure are formed from conductive material.

59. A semiconductor device according to claim 58, wherein:

the first reinforcing structure includes a first conductive material, the first conductive material being encompassed by a cover metal layer.

60. A semiconductor device according to claim 59, wherein:

the first reinforcing structure and the second reinforcing structure include a conductive material selected from a group consisting of Ni, Cu, Pd, Pt and Au; and

the cover metal layer includes a conductive material selected from a group consisting of Ni, Cu and Au.